## Yufei Shi

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## Education

Carnegie Mellon University	Pittsburgh, PA
M.S. in Electrical and Computer Engineering	. Expected May 2025
B.S. in Electrical and Computer Engineering with University Honors, CQPA: 3.69	May 2024
• Teaching assistant: Intro to Computer Systems (4 semesters); Computer Systems and HW-SW Inter-	erface (1 semester)
Courses: Intro to Computer Architecture, Parallel Computer Architecture & Programming, OS Des	ign & Implementation
Experience	
Carnegie Mellon University, ABSTRACT Research Group	Pittsburgh, PA
Research Assistant	. Jan 2023 — Present
• Conducted research on the <b>memory consistency model x</b> and <b>asynchronous program</b> Coarse-Grained Reconfigurable Architecture (CGRA), a hardware dataflow architecture.	mming model " of
Added support for lightweight threads in the dataflow execution simulator by extending the cessing element, implementing thread dispatch synchronization, and resolving legacy bugs	ISA with a new pro- within the simulator.
Analyzed CGRA's memory consistency model by developing testing programs with diverse terns, tracing their execution on the simulator and identifying violations of sequential constants.	memory access pat- sistency in the trace.
<b>T</b> Designed a HW-SW solution for <b>enforcing sequential consistent execution</b> of pipelined	l dataflow programs.
<b>G</b> Contributed to the design of a programming language for expressing parallelism in CGRA verting algorithms with irregular memory access patterns into pipelined, work-queue-base	applications by con- d implementations.
G Contributed to the implementation of a state-machine for synchronizing asynchronously-dis	spatched task inputs.
Projects	
Unix-like x86 OS Kernel with Thread Library   C, Simics	Sep-Dec 2023
• Designed and implemented a Unix-like x86 OS Kernel that supports preemptive multitaskir address spaces, and a set of important system calls as well as device drivers for timer, keyb	ng, multiple memory oard, and console.
• Implemented kernel thread context switching, scheduler with multiple scheduling queues as robin scheduling algorithm, and kernel-level synchronization primitives to realize <b>preemp</b>	nd prioritized round- tive multitasking.
• Implemented standard 32-bit x86 two-level paged virtual memory that supports zero-filled	l on-demand paging.
• Implemented <b>task/thread interface</b> that works with my implementation of a POSIX-like	thread library.
Parallel Mesh Collision Detector   C++, CUDA, GDB, OpenMP, Open3D	Apr-May 2023
• Developed a parallel algorithm to <b>accurately determine the minimum distances betwe</b> which can be used to detect potential collisions between objects in real-time for robotic models.	<b>en convex meshes</b> , otion planning tasks.
• Implemented Gilbert-Johnson-Keerthi algorithm and optimized it by parallelizing its support	rt function in CUDA.
• Developed a simulation and visualization framework for demonstrating the algorithm running	ng in complex scenes.
• Achieved a 20x speedup over the baseline by combining CUDA and OpenMP with additional terms of the second s	ional optimizations.
In-Order 2-Way Superscalar RISC-V Processor   C++, SystemVerilog, Synopsys VCS & DC	Jan-Apr 2023
• Designed and implemented an RV32I processor featuring a 2-way superscalar in-order 5-st	age pipeline.
• Implemented <b>branch prediction</b> and <b>data forwarding</b> capabilities to alleviate data ha pipeline, and ensured their integration with the final superscalar pipeline to maximize IPC	zards in the 5-stage of the processor.
• Conducted <b>timing and power optimizations</b> over design iterations by iteratively analyz and making adjustments to the design; achieved a 15% IPS increase while reducing power of	ring synthesis report consumption by 80%.
Skills	

**Programming Languages**: C, C++, Python, Rust, Shell, x86 Assembly, Common Lisp (a little bit) **Hardware Design Tools**: SystemVerilog, Synopsys VCS, Synopsys Design Compiler, Intel Quartus, Fusion 360 **Developer Tools**: GDB, Git, Make, Valgrind, awk, vim, Regex, Conda, Various Linux Distros, Pin Tool, gem5 **Technologies**: MATLAB, SOLIDWORKS, NumPy, Matplotlib, OpenMP, MPI, CUDA, OpenGL, HTML, LATEX